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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,484	11/25/2003	Byoung-Chan Kim	053933-5058	4365

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,484	KIM ET AL.	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *9-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/25/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/720484 Attorney's Docket #: 053933-5058
Filing Date: 11/25/2003; claimed foreign priority to 9/4/2003

Applicant: Kim et al.

Examiner: Alexander Williams

Applicant's election of Group I (claims 1 to 8), filed 8/27/2004, has been acknowledged.

This application contains claims 9 to 11 drawn to an invention non-elected without traverse.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The disclosure is objected to because of the following informalities: On page 19, line 10; page 26, line 23; and page 28, line 25, it is unclear what is meant by "sawn".

Appropriate correction is required.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 3 to 5 to 7 are rejected under 35 U.S.C. § 102(e) as being anticipated by Corisis et al. (U.S. Patent Application Publication # 2003/0189257).

1. Corisis et al. (figures 1 to 13) specifically figure 8 show a ball grid array (BGA) package 50 having a semiconductor chip 20a',20b' with edge-bonding metal patterns (45, see figure 1) formed thereon, comprising: a substrate 52 having circuit patterns for electric connection formed therein (inherit); a center-bonding type semiconductor chip 20a',20b' attached to the substrate, the semiconductor chip having center-bonding pads (34, see figure 1) formed on one side thereof; edge-bonding metal patterns (45, see figure 1) electrically connected to the center-bonding pads of the semiconductor chip, the edge bonding metal patterns being extended towards the edge regions of the center-bonding type semiconductor chip; connection members 56 for electrically connecting the edge bonding metal patterns extended towards the edge regions of the semiconductor chip to the circuit patterns of the substrate, respectively; a sealing material 58 for molding the substrate to protect the semiconductor chip; and solder balls (shown at the bottom of 52) attached to solder pads (not shown, but inherit) electrically connected to the circuit patterns of the substrate, respectively, for transmitting electric signals from the semiconductor chip to an external substrate.

2. Corisis et al. (figures 1 to 13) specifically figure 8 show a ball grid array (BGA) package **50** having semiconductor chips **20a',20b'** with edge-bonding metal patterns **(45, see figure 1)** formed thereon, comprising: a substrate **52** having circuit patterns for electric connection formed therein; a first center-bonding type semiconductor chip **20a'** attached to the substrate, the first semiconductor chip having center bonding pads **(34, see figure 1)** formed on one side thereof; edge-bonding metal patterns **(45, see figure 1)** electrically connected to the center-bonding pads of the first semiconductor chip, the edge-bonding metal patterns being extended towards the edge regions of the first center-bonding type semiconductor chip; a bonding member **(49, see figure 5)** applied to the first semiconductor chip to form a stacked structure; a second center-bonding type semiconductor chip **20b'** stacked on the first semiconductor chip via the bonding member, the second semiconductor chip having center-bonding pads **(34, see figure 1)** formed on one side thereof; edge-bonding metal patterns **(45,**

see figure 1) electrically connected to the center-bonding pads of the second semiconductor chip, the edge-bonding metal patterns being extended towards the edge regions of the second center-bonding type semiconductor chip; connection members **56** for electrically connecting the edge bonding metal patterns of the first and second semiconductor chips to the circuit patterns **(inherit)** of the substrate, respectively; a sealing material **58** for molding the substrate to protect the first and second semiconductor chips; and solder balls **(shown on the bottom of 52)** attached to solder pads **(inherit)** electrically connected to the circuit patterns of the substrate, respectively, for transmitting electric signals from the first and second semiconductor chips to an external substrate.

3. The package as set forth in claim 2, Corisis et al. show wherein the bonding member **(49, see figure 5)** applied to the first semiconductor chip is a nonconductive bonding agent having spacers therein, the bonding member serving to maintain balance between the first semiconductor chip and the second semiconductor chip and to prevent shorts between the second semiconductor chip and the connection members of the first semiconductor-chip.

5. The package as set forth in claim 1 or 2, Corisis et al. show wherein the connection members **56** are conductive wires.

6. The package as set forth in claim 1, Corisis et al. show wherein the edge-bonding metal patterns **(45, see figure 1)** are connected to the corresponding circuit patterns of the substrate **52** at the edge regions of the semiconductor chip **20a',20b'** by means of the connection members **56**.

7. The package as set forth in claim 2, Corisis et al. show wherein the edge-bonding metal patterns **(45, see figure 1)** are electrically connected to the corresponding circuit patterns (inherit) of the substrate **52** at the edge regions of the first and second semiconductor chips **20a',20b'** by means of the connection members **56**, respectively.

Initially, and with respect to claim 4, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over in Corisis et al. (U.S. Patent Application Publication # 2003/0189257).

As to the grounds of rejection under section 103, see MPEP § 2113.

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Corisis et al. (U.S. Patent Application Publication # 2003/0189257) in view of Miyagawa (U.S. Patent # 6,780,023).

Corisis et al. show the features of the claimed invention as detailed above, but fail to explicitly show wherein the sealing material is synthetic resin.

Miyagawa is cited for showing printed circuit board having plurality of conductive patterns passing through adjacent pads. Specifically, Miyagawa (figures 1 to 6) specifically figure 6 discloses wherein the sealing material **17** is synthetic resin for the purpose of protecting a printed circuit board surface which permits passing a plurality of conductive patterns between adjacent pads without complicating the pad shape and layout.

(3) FIG. 1 shows a circuit module 11 used in an electric apparatus such as a portable computer. The circuit module 11 comprises a ball grid array (BGA) type semiconductor package 12 and a printed wiring board 13.
(4) The semiconductor package 12 constitutes a surface mount circuit component. The semiconductor package 12 comprises a package substrate 14, an IC chip 15 and a plurality of solder balls 16. The package substrate 14 has a first surface 14a and a second surface 14b as a terminal

surface. The second surface 14b is the opposite side of the first surface 14a. The IC chip 15 is mounted on the first surface 14a of the package substrate 14, and is covered by a synthetic resin mold material 17.

Therefore, it would have been obvious to one of ordinary skill in the art to use Miyagawa's synthetic resin to modify Corisis et al.'s sealing material for the purpose of protecting a printed circuit board surface which permits passing a plurality of conductive patterns between adjacent pads without complicating the pad shape and layout.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/777,686,723,685,200,698,696,690,691	11/6/04
Other Documentation: foreign patents and literature in 257/777,686,723,685,200,698,696,690,691	11/6/04
Electronic data base(s): U.S. Patents EAST	11/6/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
11/5/04